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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,474	02/20/2004	Jian-Shen Yu	B-5381 621721-5	7461

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

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04/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,474	YU ET AL.	
	Examiner	Art Unit	
	STEPHEN G. SHERMAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4 and 8-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4 and 8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 15 February 2008. Claims 4 and 8-12 are pending.

Response to Arguments

2. Applicant's arguments filed with respect to claims 4 and 8-12 have been fully considered but they are not persuasive.

On page 6 of the response the applicant presents arguments against the rejection of claims 4 and 8-12 using Itakura (US 5,252,957). Specifically, the applicant focuses on Figure 1 of Itakura, pointing out that transistors MS and MC are coupled together and are also coupled to different inverters, and then continues by pointing out that the applicant's claims state that the first and second TFTs are coupled to the same inverter. The examiner generally agrees with the statements made by the applicant regarding their claims and Figure 1 of Itakura, however, the applicant has completely ignored the rejection made by the examiner. In the examiner's rejection, Figure 1 was not what was used to show the feature of the transistors MC and MS being coupled to the same inverter. The examiner used Itakura's prior art explanation found in column 1 for the basis of the rejections (See the rejection below). The examiner then explicitly points out in the rejection of the claims that in Column 4, lines 41-50, where Itakura is explaining the configuration of Figure 1, Itakura states that "The basic construction is

the same as the conventional construction. However, a sampling pulse different from a sampling pulse input to the gate of the first field effect transistor MS is applied to the gate of the second field effect transistor MC..." This means that in the convention example explained in Column 1 of Itakura the inverter INV shown in Figure would have been connected to the same stage instead of the next stage, which means that the transistors would have been connected to the same inverter as the claims require. Figure 1 of Itakura was only used in the rejection as an example, since Itakura explains the only difference in column 4, lines 41-50, to physically show the configuration of the prior art described in column 1 since Itakura did not provide a Figure of the prior art. Therefore, Itakura anticipates the claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 4 and 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Itakura (US 5,252,957).

Regarding claim 4, Itakura discloses a sampling circuit for an analog signal according to a clock signal, comprising:

a first thin film transistor (Column 1, lines 27-30),

having a first electrode to receive the analog signal, a control electrode to receive the clock signal and a second electrode for sampling the analog signal when the clock signal is at a first logic level (Column 1, lines 27-30 explain that the transistor samples a video signal, i.e. analog signal, and column 1, lines 60-61 explain that this is done when a sampling pulse, i.e. clock signal, is supplied to the transistor. Furthermore, column 4, lines 41-50 explains that Figure 1 is the same as the conventional example described in column 1 except that in the conventional example the same sampling pulse is applied to the first transistor and the inverter. Thus, looking at Figure 1, it can be seen that transistor MS receives and analog signal at a first electrode, and samples the analog signal using the second electrode when a sampling signal is sent at a first logic level to the control electrode.); and

a counteracting device coupled to the second electrode and comprising:

an inversion device (Column 1, line 47), having an input terminal coupled to the control electrode (Column 4, lines 41-50 explains that Figure 1 is the same as the conventional example described in column 1 except that in the conventional example the same sampling pulse is applied to the first transistor and the inverter. Thus, looking at Figure 1, it can be seen that the inversion device has an input terminal coupled to the control electrode of the first TFT.); and

a second TFT (Column 1, lines 33-39) having a gate terminal coupled to an output terminal of the inversion device and a source and drain terminal both coupled to the second electrode (Column 4, lines 41-50 explains that Figure 1 is the same as the

conventional example described in column 1 except that in the conventional example the same sampling pulse is applied to the first transistor and the inverter. Thus, looking at Figure 1, it can be seen that TFT MC has a gate coupled to the output of the inverter INV and that the source and drain are coupled together and are each coupled to the second electrode of transistor MS.);

wherein when the clock signal is changed from the first logic level to a second logic level, the capacitor reduces the feed-through voltage drop caused by a parasitic capacitor between the second electrode and the control electrode of the first TFT (Column 1, lines 39-43 explain that the second transistor is for charge compensation, where the excess charges include feed-through charges, i.e. feed through voltage, entering from the gate, i.e. control electrode, of the TFT. Regardless, the examiner understands that since the structure of Itakura is the same as the structure in the specification, the circuit of Itakura will inherently reduce the feed-through voltage drop caused by a parasitic capacitance when the transistor MS is turned on/off by the sampling signal.).

Regarding claim 8, please refer to the rejection of claim 4, and furthermore Itakura also discloses:

a plurality of display units, arranged in array (Column 4, lines 41-50 explains that Figure 1 is the same as the conventional example described in column 1 except that in the conventional example the same sampling pulse is applied to the first transistor and the inverter. Then column 4, lines 12-17 explain that Figure 2 shows the whole

construction of the LCD using the driving circuit shown in Figure 1. Thus, looking at Figure 2, it can be seen that there are a plurality of display units shown as elements 2.);

a plurality of data lines disposed corresponding to each line of the display units, wherein each data line provides a video signal to the corresponding display unit (Figure 1 shows data lines at the outputs of the sample and hold circuits.); and

a data driving circuit (Figure 1), having at least the sampling circuit described in claim 4 (Figure 1 shows the S/H circuits.).

Regarding claim 9, please refer to the rejection of claim 4, and furthermore Itakura also discloses of the counteracting device having a capacitor between the second electrode and an output terminal of the inversion device (Column1, lines 43-50 explain that the transistor is a capacitor, where the transistors is between the second electrode and output of the inverter [see Figure 1].).

Regarding claim 10, Itakura discloses the circuit as claimed in claim 9, wherein the first TFT is an NMOS transistor (Column 1, lines 27-30 explain that the first transistor is a MOS transistor, which is shown in Figure 1 to be N-type.).

Regarding claim 11, please refer to the rejection of claim 8, and furthermore Itakura also discloses of the counteracting device having a capacitor between the second electrode and an output terminal of the inversion device (Column1, lines 43-50

explain that the transistor is a capacitor, where the transistors is between the second electrode and output of the inverter [see Figure 1].).

Regarding claim 12, this claim is rejected under the same rationale as claim 10.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN G. SHERMAN whose telephone number is (571)272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen G Sherman/
Examiner, Art Unit 2629

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

17 April 2008